WHAT IS CLAIMED IS:

1. A method for manufacturing a buried strap contact between a transistor and a trench capacitor in a memory cell, comprising:

a) generating a trench capacitor in a substrate, the trench capacitor comprising a lower region filled with a first doped filler material having a first width and comprising an open, unfilled region adjacent to it, the unfilled region comprising sidewalls and a floor formed by the first doped filler material;

b) filling the unfilled region of the trench capacitor with essentially monocrystalline silicon;

c) generating gate paths on the substrate surface;

d) etching, for generating a buried strap contact, a contact trench having a second width at least down to a depth of the floor formed by the first doped filler material, the gate paths forming at least part of a mask utilized for etching the contact trench;

e) depositing a second filler material in the contact trench for forming a buried bridge as part of the buried strap contact, the buried bridge being in direct contact with the first doped filler material; and

f) providing at least one thermal treatment in order to generate a diffusion region as part of the buried strap contact.

2. The method according to claim 1, wherein the memory cell is a DRAM memory cell.

3. The method according to claim 1, further comprising:

applying a first insulation layer on the floor of the opened, unfilled region before stage b).

4. The method according to claim 3, wherein the first insulation layer is a silicon oxide layer.

5. The method according to claim 1, wherein the second width of the contact trench is less than the first width of the filled region of the trench capacitor.

6. The method according to claim 1, wherein the first doped filler material is polysilicon with a dopant.

7. The method according to claim 6, further comprising providing As or P as a dopant, preferably in a dopant concentration of 10^{19} through 10^{20} cm^{-3}.

8. The method according to claim 1, further comprising providing the dopant in a concentration of 10^{19} through 10^{20} cm^{-3}.

9. The method according to claim 1, further comprising providing polysilicon as second filler material.

10. The method according to claim 1, further comprising providing lateral spacers for the gate paths.

11. The method according to claim 1, further comprising filling the unfilled region of the trench capacitor with monocrystalline silicon in stage b) utilizing an epitaxial deposition method.

12. The method according to claim 11, wherein the epitaxial deposition method is a CVD method.

13. The method according to claim 1, wherein the substrate comprises a trench insulation that forms at least one sidewall of the open, unfilled region of the trench capacitor.